AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Withdrawn): A method of manufacturing an electronic parts packaging structure, comprising the steps of:

forming a first resin film uncured on a wiring substrate including a wiring pattern;

burying an electronic parts having a connection terminal on an element formation surface in the first resin film uncured in a state where the connection terminal is directed upward;

forming a second resin film for covering the electronic parts;

obtaining an insulation film by curing the first and second resin films by heat treatment;

forming a via hole in a predetermined portion of the insulation film on the wiring pattern and the connection terminal; and

forming an upper wiring pattern connected to the wiring pattern and the connection terminal through the via hole, on the insulation film.

Claim 2 (Withdrawn): A method of manufacturing an electronic parts packaging structure, comprising the steps of:

forming a resin film uncured on a wiring substrate including a wiring pattern;

burying an electronic parts, which has a connection terminal and a passivation film having an opening portion for exposing the connection terminal on an element formation surface, in the resin film uncured in a state where the connection terminal is directed upward;

obtaining an insulation film by curing the resin film by heat treatment;

forming a via hole in a predetermined portion of the insulation film on the wiring pattern; and

forming an upper wiring pattern, which is connected to the wiring pattern through the via hole and connected to the connection terminal through the opening portion, on the insulation film and the electronic parts.

Claim 3 (Withdrawn): A method of manufacturing an electronic parts packaging structure, comprising the steps of:

forming a resin film uncured on a wiring substrate including a wiring pattern;

burying an electronic parts having a connection terminal on an element formation surface in the resin film uncured in a state where the connection terminal is directed downward, and joining the connection terminal to the wiring pattern;

obtaining an insulation film by curing the resin film by heat treatment;

forming a via hole in a predetermined portion of the insulation film on the wiring pattern; and

forming an upper wiring pattern connected to the wiring pattern through the via hole, on the insulation film.

Claim 4 (Withdrawn): A method of manufacturing an electronic parts packaging structure, comprising the steps of:

forming a first resin film uncured on a wiring substrate including a wiring pattern;

burying an electronic parts having a connection terminal on an element formation surface in the first resin film uncured in a state where the connection terminal is directed downward, and joining the connection terminal to the wiring pattern;

forming a second resin film for covering the electronic parts;

obtaining an insulation film by curing the first and second resin films by heat treatment;

forming a via hole in a predetermined portion of the insulation film on the wiring pattern; and

forming an upper wiring pattern connected to the wiring pattern through the via hole, on the insulation film.

Claim 5 (Withdrawn): The method according to any one of claims 3 and 4, after the step of forming the resin film uncured and before the step of joining the connection terminal of the electronic parts to the wiring pattern, further comprising the step of:

forming an opening portion in a portion of the resin film on the wiring pattern to which the connection terminal of the electronic parts is joined,

wherein the step of joining the connection terminal of the electronic parts to the wiring pattern includes placing the connection terminal of the electronic parts while making the connection terminal of the electronic parts correspond to the opening portion of the resin film.

Claim 6 (Withdrawn): The method according to claim 5,

wherein the connection terminal of the electronic parts is a solder bump, and

wherein in the step of joining the connection terminal of the electronic parts to the wiring pattern, a gap between the electronic parts and a side surface of the opening portion of the resin film is filled by deforming the solder bump by reflowing and curing.

Claim 7 (Withdrawn):. The method according to any one of claims 1 to 4, wherein in the step of burying the electronic parts in the resin film uncured, an upper surface of the resin film uncured and any one of the element formation surface and a backside of the electronic parts are set at an almost same height.

Claim 8 (Withdrawn): The method according to any one of claims 1 and 2, wherein in the step of burying the electronic parts in the resin film uncured, the resin film is interposed between a backside of the electronic parts and the wiring substrate.

Claim 9 (Withdrawn): The method according to claim 3, wherein in the step of forming the upper wiring pattern, the upper wiring pattern is not formed on the electronic parts.

Claim 10 (Withdrawn): The method according to any one of claims 1 to 4, further comprising the step of: repeating the steps from the step of burying the electronic parts in the resin film to the step of forming the upper wiring pattern with a predetermined number of times.

Claim 11 (Withdrawn): The method according to any one of claims 1 to 4, further comprising the step of, flip-chip bonding an upper electronic parts to the upper wiring pattern.

Claim 12 (Withdrawn): The method according to any one of claims 1 to 4, wherein the electronic parts is a semiconductor chip having a thickness of approximately 150 μm or less.

Claim 13 (Currently Amended): An electronic parts packaging structure comprising:

a wiring substrate including a wiring pattern;

a first insulation film formed on the wiring substrate;

an electronic parts having a connection terminal on an element formation surface, the electronic parts being buried in the first insulation film in a state where the connection terminal is directed upward and being mounted in a state where ~~a backside of the electronic parts is not in contact with the wiring substrate and~~ a lower portion of the first insulating film exists between the electronic parts and the wiring substrate, and the back side of the electronic parts is electrically insulated with the wiring substrate by the lower portion of the first insulation film;

a second insulation film for covering the electronic parts, and whose upper surface is flat over a whole on the wiring substrate, and the second insulation film contacting with the electronic parts as a single layer, and;

first via holes formed in a predetermined portion of the first and second insulation films on the wiring pattern, and having an identical inner surface;

second via holes formed in a portion of the second insulating film on the connection terminal of the electron parts;

via holes respectively formed in a predetermined portion of the first and second insulation films on the wiring pattern and the connection terminal;

an upper wiring pattern ~~formed~~ as a single wiring formed on the second insulation film, the upper wiring pattern being connected to the wiring pattern and the connection terminal through the via holes, wherein, the electronic parts is electrically connected to the wiring pattern of the wiring substrate by only the upper wiring pattern; and

an upper electronic part [[with]] whose bumps ~~which~~ are flip-chip bonded to connection portions of the upper wiring pattern, the connection pad which directly contacts the upper surface of the second insulating film.

Claim 14 (Withdrawn): An electronic parts packaging structure comprising:

a wiring substrate including a wiring pattern;

an insulation film formed on the wiring substrate;

an electronic parts including a connection terminal and a passivation film having an opening portion for exposing the connection terminal on an element formation surface, the electronic parts being buried in the insulation film in a state where the connection terminal is directed upward and being mounted in a state where a backside of the electronic parts is not in contact with the wiring substrate;

a via hole formed in a predetermined portion of the insulation film on the wiring pattern; and

an upper wiring pattern formed on the insulation film and the electronic parts, the upper wiring pattern being connected to the wiring pattern through the via hole and connected to the connection terminal through the opening portion.

Claim 15 (Previously Presented): The electronic parts packaging structure according to claims 13 or 14, wherein the element formation surface of the electronic parts and an upper surface of the insulation film in which the electronic parts is buried are at an almost same height to be planarized.

Claim 16 (Previously Presented): The electronic parts packaging structure according to claims 13 or 14, wherein the electronic parts is a semiconductor chip having a thickness of approximately 150 μm or less.

Claim 17 (Previously Presented): The electronic parts packaging structure according to claims 13 or 14, wherein the insulation film is made of resin.